UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/524,408	03/13/2000	Kanad Chakraborty	YO999-598	7403

21254 7590 09/24/2003

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	7

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/524,408	CHAKRABORTY ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2000, and 5/25/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: METHOD AND APPARATUS FOR APPLYING FINE GRAINED TRANSFORMS DURING PLACEMENT SYNTHESIS INTERACTION
2. First named inventor is: CHAKRABORTY
3. Claims 1-39 have been submitted, examined, and rejected.
4. The independent claims are: 1, 16, 21, 22, 37-39.
5. This is the first office action on the merits, and is non-final.
6. US Application was filed 03/13/00, and there are no claims for earlier priority.

Index of Prior Art

7. Shenoy refers to US Patent 6,378,114.

Specification and Drawings

8. A discussion of the specification and drawings is useful as a support for the 35 USC 112 rejections, because most of the enablement and indefinite rejections spring from a common theme. The common theme is simultaneous optimization of multiple domains, which is repeatedly claimed with slightly varying terminology. It appears efficient to discuss simultaneous optimization in detail now, rather than repeating the entire discussion for each 35 USC 112 rejection.
9. THREE SEPARATE DOMAINS. Applicant presents an interesting broad conceptual approach to integrated circuit design, whereby the circuit design space is defined by three separate domains, "in Figure 1, the three axes represent optimizations along Boolean, electrical and physical domains" at specification page 5 lines 3-4. Said broad conceptual approach is useful for broad conceptual or theoretical discussions.
10. However, Applicant's representation of circuit design space is a bit simplistic in a practical sense, because the three domains interact in a complex, non-linear, and unpredictable fashion. Optimizing in one domain generally degrades another domain. For example, circuit elements (transistors) with larger areas are faster (electrical domain), but take more layout area (physical domain). Thus, Applicant's representation of the prior art's sequential optimization as traveling sequentially from point to point in directions parallel with the axes

(specification page 5 and FIG 1 points A-F) is not fully accurate because the axes are interactive.

11. Note that optimization in a single domain will simultaneously affect the other domains. For example, the electrical and physical domains are directly related, as discussed in the transistor example above. The Boolean domain is slightly different because the electrical and physical domains may be changed without changing the Boolean domain. However, any change in the Boolean domain will always change both the physical and electrical domains.
12. Further, at specification page 9 line 17, Applicant asserts that "a single step may optimize the physical, Boolean and electrical dimensions, thus moving the design from point A to F' in the design space. Multiple steps are not required". This broad assertion is not supported. For example, first the Boolean space is changed, then this change is propagated to the electrical domain (new electrical elements to implement the new Boolean logic, and new basic characteristics of the new electrical elements), and then propagated to the physical (layout) domain, and then propagated to the electrical domain again (capacitance of connecting lines, noise from connecting lines, and related electrical characteristics that are dependent upon the layout of the electrical elements). **This simple example illustrates the point that changes to a single domain must be propagated sequentially to the other domains.**
13. Thus, simultaneous (or "concurrent") optimization in multiple domains is repeatedly claimed, but is not adequately supported by the specification.
14. COMPLEXITY OF INTEGRATED CIRUITS. Modern integrated circuits are probably the most complex creations of man. They contain millions of individual electrical elements, tightly packed into three dimensions, with electric charges generating electric fields, and with moving charges generating magnetic fields, with heat being generated and dissipated, with logical operations occurring, and with all of these chemical, electrical, logical, quantum semiconductor, and thermal phenomenon interacting in space and in time at frequencies of millions or billions of cycles per second. Thus, the design of integrated circuits is highly unpredictable. See the Wands 8 factor test regarding undue experimentation, particularly factor (7) "the predictability or unpredictability of the art", *In re Wands* (CA FC) 8 USPQ2d 1400, 1404 (9/30/1998).

Claim Rejections - 35 USC § 112- first paragraph- enablement

15. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. **Claims 1, 5, 9-10, 15, 16-18, 21, 22, 26, 30-31, 36, 38, and 39** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

17. Claim 1 states "**optimize the netlist and placement properties concurrently".** Webster defines "concurrent" as "operating or occurring at the same time". It does not appear possible to optimize the netlist and the placement properties simultaneously. For example, using larger transistors increases the speed (electrical domain), but unfortunately also increases the layout area (physical domain). The relationship between netlist and placement is complex, and non-linear, and not predictable.

18. Claim 5 states "**a single transform selectively optimizes** the physical, Boolean and electrical domains", and is not enabled for the same reasons as claim 1.

19. Claim 9 states **"utilizing an infrastructure of bins, and wherein a timing, congestion and noise analysis is based on the bins".** Congestion analysis based upon bins is enabled, but the specification does not enable timing and noise analysis based upon the bins. Note that timing requires the netlist and the electrical properties of the elements, and cannot be analyzed based upon the bins. Further, the exact wiring layout also affects capacitance, and thus affects the timing. Similarly, the noise cannot be analyzed based upon the bins. However, the congestion could be analyzed based upon the bin area utilization.

20. Claim 10 states **"placement and netlist changes are performed together in said fine-grained transforms",** and is not enabled for the same reasons as claim 1.

21. Claim 15 states "synthesis, timing, and placement data are concurrently available to all of said transforms, such that said **transforms modify a netlist and placement concurrently",** and is not enabled for the same reasons as claim 1.

22. Claim 16 states **"applying transforms the change the physical, electrical and Boolean logic design space concurrently",** and are not enabled for the same reasons as claim 1.
23. Claim 17 states **"design convergence".** Webster defines "converge" as "to tend or move toward one point or another... to approach a limit". As previously discussed, the physical, electrical and Boolean logic design domains have complex, non-linear, and unpredictable relationships. The specification does not enable simultaneous convergence in the three domains.
24. Claim 18 states **"considering concurrently subsets of fine-grained Boolean transforms, electrical transforms, and physical transforms",** and is not enabled for the same reasons as claim 1.
25. Claim 21 states **"applying transforms that change the physical, electrical and Boolean space concurrently... until design convergence",** and is not enabled for the same reasons as claim 1 and claim 17.
26. Claims 22, 26, 30-31, and 36 are "system" claims with the same limitations as "method" claims 1, 5, 9-10, and 15 respectively, and thus are not enabled for the same reasons respectively.
27. Claim 38 states **"converging design flow process... optimize... concurrently",** and is not enabled for the same reasons as claim 1 and claim 17.
28. Claim 39 states **"transforms that change the physical, electrical and boolean space concurrently",** and is not enabled for the same reasons as claim 1.

Claim Rejections - 35 USC § 112-Second Paragraph-indefinite claims

29. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
30. **Claims 1, 3-6, 8, 11-14, 17, 19, 20, 22, 24-27, 29, 32-35, and 37** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
31. Claims 1, and 37 state **"selectively applying a set of more and less granular placement and netlist modification transforms".** The specification does not adequately describe the term "more and less granular". Specification page 6 line 8 states "single fined-grained step

which may comprise of multiple objectives and constraints which involve both physical (placement), electrical and logical data".

32. Further, specification page 16 line 22 states "a fine-grained transform unit 308 for placing sizeless cells which have only gain values assigned to them". Also, specification page 14 line 11 states "bins... hold logic and a rough (course) representation of where the chip is (or should be located)".
33. It is not clear whether the claim 1 term "more and less granular placement" refers to these sections of the specification, and these sections of the specification appear contradictory. Please clarify.
34. Further, it is not clear what is meant by the term "more and less", because something cannot be more and less at the same time. Possibly the applicant intended the common phrase "more or less". Possibly Applicant intended a sequential application of transforms, some "more" and some "less". In any case, Applicant's intent is not clear.
35. Similarly, claims 1, 3, 4, 6, 16, 21, 37, 38, 39 state **"fine-grained",** which is not adequately defined. Note that specification page 16 refers to "sizeless cells", but page 6 refers to "physical (placement)". Again, these sections appear contradictory.
36. Claim 3 states "**a function of said placement and synthesis transforms are decomposed into a set of fine-grained transforms each addressing a specific phase of the placement and synthesis process".** The terms "a function" and "decomposed" are not adequately defined. Further, it is not clear whether the "decomposed" refers to the "function", or refers to the transforms composing the function.
37. Claim 4 states **"selectively mixed and matched predetermined".** This term is not adequately defined, it is not clear how selections are made.
38. Claim 5 states "a single transform **selectively optimizes** the physical, Boolean and electrical domains". It is not clear how the single transform "selectively" optimizes three domains simultaneously. Note the term "simultaneously" in the preamble of claim 1, which is the base claim of claim 5.
39. Claim 6 states "**a single fine-grained transform** includes multiple objectives and constraints which involve physical placement and logical data. It is not clear how a single transform can

include multiple objectives and constraints involving both physical placement and logical data.

40. Claim 8 states **"a single converging flow of fine grained operations".** Webster defines "converge" as "to tend or move toward one point or another... to approach a limit". As previously discussed, the physical, electrical and Boolean logic design domains have complex, non-linear, and unpredictable relationships. It is not clear what "convergence" means with respect to optimizing the three domains.
41. Claim 11 states **"said fine-grained transforms are organized together in flexible scenarios to create a design closure process".** It is not clear what "organized together in flexible scenarios" means. Also, it is not clear what "design closure" means. See the discussion of "design convergence" in claim 17 below.
42. Claim 12 states **"at predetermined stages of the process, selectively determining whether to intercept the process and implement any of a plurality of fine-grained transforms".** It is not clear which stages are predetermined, it nor it is clear how the selective determination is made, nor is it clear how to "intercept" a process.
43. Claim 13 states "**examining a plurality of domains concurrently in finding an optimum design, said examining comprising creating a sequence of more and less granular placement and netlist transforms, to create a converging design closure process**". Claim 13 is indefinite for the same reasons as claim 1, claim 17.
44. Claim 14 states **"all transforms have a unified view of the placement and synthesis design space".** It is not clear what "unified view" means in this context.
45. Claim 17 states "**design convergence".** Webster defines "converge" as "to tend or move toward one point or another... to approach a limit". As previously discussed, the physical, electrical and Boolean logic design domains have complex, non-linear, and unpredictable relationships. It is not clear what "convergence" means with respect to optimizing the three domains.
46. Claim 19 states **"blocks of each of the boolean optimizations, electrical optimizations and physical optimizations are interspersed together".** The term "interspersed" appears to imply sequential transformations, however, the preamble of claim 1 states "applying transforms for simultaneously modifying a plurality of domains". Thus, the implied

sequential transformation of claim 19 appear contradictory to the "simultaneously" of base claim 1.

47. Claim 20 states **"each of said optimizations is represented as a plurality of transformations and that the optimizations are divided and interspersed together, to examine each of the Boolean, electrical and physical domains concurrently".** Claim 20 is indefinite for the same reasons as claim 19.
48. Claims 22, 24-27, 29, 32-35 are "system" claims with the same limitations as "method" claims 1, 3-6, 8, 11-14 respectively, and thus are indefinite for the same reasons respectively.
49. Claim 37 is indefinite for the same reasons as claim 1.

35 USC § 102(e): filed before 11/29/00 and not vol. pub. under 35 USD 122(b)

50. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
51. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).
52. **Claims 1, 2, and 7 are rejected under 35 U.S.C. 102(e)** as anticipated by Shenoy US Patent 6,378,114.
53. Claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.
54. Claim 1 is an independent "method" claim with 2 limitations, labeled by the Examiner for clarity.
55. A-**"selectively applying a set of more and less granular placement and netlist modification transforms separately or in a flexible sequence to create a converging design process flow"** is disclosed by Shenoy at column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

56. B-"**wherein said transforms comprise fine-grained steps to optimize the netlist and placement properties of a design concurrently**" is disclosed by Shenoy at column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
57. Claim 2 is rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.
58. Claim 2 depends from Claim 1, with 1additional limitations.
59. **"said creating starts from a netlist without an initial placement of said circuit or from a netlist with an initial placement"** is disclosed by Shenoy at column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
60. Claim 7 is rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.
61. Claim 7 depends from claim 1, with 1 additional limitation.
62. **"a partially placed and synthesized design is a starting point of said creating"** is disclosed by Shenoy at column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

Conclusion

63. All claims 1-39 stand rejected.

Communication

64. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM.
65. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are: (703) 872-9306 for official communications; and (703) 746-7240 for non-official or draft communications.
66. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER